What is claimed is:

1   1.   A test chip, comprising:

2   at least one level having an m x n array of regions, where m and n are integers, each

3   region capable of including at least one test structure, at least some of the regions including

4   respective test structures,

5   the level having m+1 driver lines oriented in a first direction, the m+1 driver lines

6   connected to collectively provide input signals to all of the test structures,

7   the level having 4n receiver lines arranged in a second direction, the 4n receiver lines

8   connected to collectively receive output signals from all of the test structures,

9   wherein the test structures are arranged and connected so that each of the structures

10   can be individually addressed for testing using the m+1 driver lines and 4n receiver lines.

1   2.   The test chip of claim 1, wherein:

2   each test structure is connected to at least one of the driver lines with a first diode,

3   transistor or controlled switch therebetween, and

4   each test structure is connected to at least one of the receiver lines with a second

5   diode, transistor or controlled switch therebetween.

1   3.   The test chip of claim 1, wherein:

2   each test structure has two inputs connected by respective diodes, transistors or

3   controlled switches to a respective two of the driver lines, and

4   each test structure has two outputs connected by respective diodes, transistors or

5   controlled switches to a respective two of the receiver lines.

1   4.   The test chip of claim 1, wherein:

2   the test structures are arranged in m columns and n rows,

3   each column has a first one of the driver lines adjacent thereto and connected thereto

4   on a first side thereof and a second one of the driver lines adjacent thereto and connected

5   thereto on a second side thereof,

6   each row has a first pair of the receiver lines adjacent thereto and connected thereto

7   on a first side thereof and a second pair of the receiver lines adjacent thereto and connected

8   thereto on a second side thereof.

1 5. The test chip of claim 1, wherein:

2 the test structures are arranged in n columns and m rows,

3 each row has a first one of the driver lines adjacent thereto and connected thereto on a

4 first side thereof and a second one of the driver lines adjacent thereto and connected thereto

5 on a second side thereof,

6 each column has a first pair of the receiver lines adjacent thereto and connected

7 thereto on a first side thereof and a second pair of the receiver lines adjacent thereto and

8 connected thereto on a second side thereof.

1 6. The test chip of claim 1, wherein:

2 the test chip has p levels with test structures, where p is an integer greater than one,

3 each of the p levels having m x n regions, at least some of the regions in each level containing

4 test structures,

5 the chip has p x (m+1) driver lines, with each test structure connected to a respective

6 at least one of the driver lines,

7 the chip has 8n receiver lines, with each test structure connected to a respective at

8 least one of the receiver lines,

9 wherein the test structures are arranged and connected so that each of the p x (m x n)

10 test structures can be individually addressed for testing using the p x (m+1) driver lines and

11 8n receiver lines.

1 7. The test chip of claim 6, wherein:

2 the p levels include odd numbered levels and even numbered levels,

3 each level has 4n receiver lines,

4 the respective commonly positioned receiver lines from each of the odd numbered

5 levels are connected to each other, and

6 the respective commonly positioned receiver lines from each of the even numbered

7 levels are connected to each other.

1 8. A test chip, comprising:

2 at least one level having an array of regions, each region capable of including at least

3 one test structure, at least some of the regions including respective test structures,

4   the level having a plurality of driver lines that provide input signals to the test

5   structures, ·

6   the level having a plurality of receiver lines that receive output signals from the test

7   structures,

8   the level having a plurality of devices for controlling current flow,

9   wherein each test structure is connected to at least one of the driver lines with a first

10   one of the devices therebetween, and

11   each test structure is connected to at least one of the receiver lines with a second one

12   of the devices therebetween, so that each of the test structures can be individually addressed

13   for testing using the driver lines and receiver lines.

1   9.   The test chip of claim 8, wherein:

2   each test structure has two inputs connected by respective devices to a respective two

3   of the driver lines, and the devices are from the group consisting of diodes, transistors and

4   controlled switches, and

5   each test structure has two outputs connected by respective devices to a respective

6   two of the receiver lines, and the devices are from the group consisting of diodes, transistors

7   and controlled switches.

1   10.   The test chip of claim 8, wherein:

2   the test structures are arranged in m columns and n rows,

3   each column has a first one of the driver lines adjacent thereto and connected thereto

4   on a first side thereof and a second one of the driver lines adjacent thereto and connected

5   thereto on a second side thereof,

6   each row has a first pair of the receiver lines adjacent thereto and connected thereto

7   on a first side thereof and a second pair of the receiver lines adjacent thereto and connected

8   thereto on a second side thereof.

1   11.   The test chip of claim 8, wherein:

2   the test structures are arranged in n columns and m rows,

3   each row has a first one of the driver lines adjacent thereto and connected thereto on a

4   first side thereof and a second one of the driver lines adjacent thereto and connected thereto

5   on a second side thereof,

6   each column has a first pair of the receiver lines adjacent thereto and connected

7   thereto on a first side thereof and a second pair of the receiver lines adjacent thereto and

8   connected thereto on a second side thereof.

1   12.   The test chip of claim 8, wherein:

2   the test chip has p levels with test structures, where p is an integer greater than one,

3   each of the p levels having regions, at least some of the regions in each level containing test

4   structures, the p levels include odd numbered levels and even numbered levels,

5   each level has commonly positioned receiver lines,

6   the respective commonly positioned receiver lines from each of the odd numbered

7   levels are connected to each other, and

8   the respective commonly positioned receiver lines from each of the even numbered

9   levels are connected to each other.

1   13.   A test chip, comprising:

2   at least one level having an array of regions with m columns and n rows, where m and

3   n are integers, each region capable of including at least one test structure, at least some of the

4   regions including respective test structures,

5   the level having $m+1$ driver lines oriented in a first direction, with the m columns

6   arranged between successive ones of the $m+1$ driver lines, each test structure having two

7   inputs connected by respective diodes, transistors, or controlled switches to a respective two

8   of the driver lines, the $m+1$ driver lines collectively providing input signals to all of the test

9   structures,

10   the level having $4n$ receiver lines oriented in a second direction, each of the n rows

11   arranged between a respective first pair of the $4n$ receiver lines on a first side thereof and a

12   respective second pair of the $4n$ receiver lines on a second side thereof, each test structure

13   having first and second outputs connected by respective diodes, transistors or controlled

14   switches to respective ones of the receiver lines on the first and second side of that test

15   structure, so that the $4n$ receiver lines collectively receive output signals from all of the test

16   structures, whereby each of the structures can be individually addressed for testing.

1   14.   The test chip of claim 13, wherein:

2   the test chip has p levels with test structures, where p is an integer greater than one,

3   each of the p levels having m x n regions, at least some of the regions in each level containing

4   test structures,

5   the chip has p x (m+1) driver lines, with each test structure connected to a respective

6   at least one of the driver lines,

7   the chip has 8n receiver lines, with each test structure connected to a respective at

8   least one of the receiver lines,

9   wherein the test structures are arranged and connected so that each of the p x (m x n)

10   test structures can be individually addressed for testing using the p x (m+1) driver lines and

11   8n receiver lines.

1   15.   The test chip of claim 14, wherein:

2   the p levels include odd numbered levels and even numbered levels,

3   each level has 4n receiver lines,

4   the respective commonly positioned receiver lines from each of the odd numbered

5   levels are connected to each other, and

6   the respective commonly positioned receiver lines from each of the even numbered

7   levels are connected to each other.

1   16.   A test chip, comprising:

2   at least one layer having n regions, where n an integer, each region capable of

3   including at least one test structure, at least some of the regions including respective test

4   structures, each comprising a nest of m parallel lines, where m is an integer,

5   the at least one layer having m driver lines, the m driver lines connected to provide

6   input signals to the respective m parallel lines in each nest,

7   the at least one layer having at least 2n receiver lines, the at least 2n receiver lines

8   connected to collectively receive output signals from all of the test structures,

9   wherein the test structures are arranged and connected to the m driver lines and at

10   least 2n receiver lines so that a presence of a short or open circuit defect in any of the nests

11   can be identified.

1   17.   The test chip of claim 16, wherein the layer has 3n receiver lines.

1   18.   The test chip of claim 16, wherein :

2   the test chip has p layers, each layer having n regions, at least some of the regions in

3   each layer including respective nests of m parallel lines,

4   each of the p layers having m driver lines, the m driver lines connected to provide

5   input signals to the respective m parallel lines in each nest in that respective layer,

6   each layer having at least 2n receiver lines, the at least 2n receiver lines connected to

7   collectively receive output signals from all of the test structures in that respective layer.

1   19.   The test chip of claim 18, wherein the receiver lines having corresponding

2   connections in each respective one of the odd numbered layers are connected to each other.

1   20.   The test chip of claim 19, wherein the test structures and receiver lines in the odd

2   numbered layers are oriented in a common direction.

1   21.   The test chip of claim 19, wherein the receiver lines having corresponding

2   connections in each respective one of the even numbered layers are connected to each other.

1   22.   The test chip of claim 21, wherein:

2   the test structures and receiver lines in the odd numbered layers are oriented in a first

3   common direction; and

4   the test structures and receiver lines in the even numbered layers are oriented in a

5   second common direction different from the first common direction.

1   23.   A test method, comprising the steps of:

2   (a)   forming circuit paths for at least one level of a chip, the level having an m x n array of

3   regions, where m and n are integers, at least some of the regions including respective test

4   structures,

5   (b)   forming m+1 driver lines oriented in a first direction, each test structure being

6   connected to at least one of the driver lines;

7   (c)   forming 4n receiver lines arranged in a second direction, each test structure being

8   connected to at least one of the receiver lines;

9   (d)   individually addressing all the test structures using the m+1 driver lines and 4n

10   receiver lines; and

11   (e)   providing input signals to all of the test structures using the m+1 driver lines, and

12   (f)   receiving output signals from all of the test structures using the 4n receiver lines.

1   24.   The test method of claim 23, wherein:

2   each test structure has two inputs connected by respective diodes, transistors or

3   controlled switches to a respective two of the driver lines, and

4   each test structure has two outputs connected by respective diodes, transistors or

5   controlled switches to a respective two of the receiver lines.

1   25.   The method of claim 23, wherein:

2   each test structure in the level is connected to at least one of the driver lines with a

3   first diode therebetween,

4   each test structure in the level is connected to at least one of the receiver lines with a

5   second diode therebetween,

6   step (e) includes performing as one of the group consisting of an inner loop and an

7   outer loop a sequence of successively applying a first signal to each driver line of the level,

8   one at a time, while applying a second signal to all remaining driver lines in the level; and

9   step (f) includes performing as the other of the group consisting of the inner loop and

10   the outer loop a sequence of measuring a current to ground at each receiver line of the level,

11   wherein the inner loop is performed each time the an iteration of the outer loop is performed.

1   26.   The method of claim 23, wherein:

2   each test structure in the level is connected to at least one of the driver lines with a

3   first transistor therebetween,

4   each test structure in the level is connected to at least one of the receiver lines with a

5   second transistor therebetween, and

6   step (e) includes performing as one of the group consisting of an inner loop and an

7   outer loop a sequence of successively applying a first voltage to each driver line of the level,

8   one at a time, while applying a second voltage to all remaining driver lines in the level;

9   step (f) includes performing as the other of the group consisting of the inner loop and

10   the outer loop a sequence of applying the second voltage to each receiver line of the level,

11   one at a time, while applying the first voltage to all remaining receiver lines in the level; and

12   the method further comprises measuring a wafer substrate current to ground each time

13   the second voltage is applied to a different receiver line in step (e).

1   27.   The test method of claim 23, wherein:

2   the chip has p levels with test structures, where p is an integer greater than one, each

3   of the p levels having m x n regions, at least some of the regions in each level containing test

4   structures,

5   the chip has p x (m+1) driver lines, with each test structure connected to a respective

6   at least one of the driver lines,

7   the chip has 8n receiver lines, with each test structure connected to a respective at

8   least one of the receiver lines, and

9   step (d) includes individually addressing the p x (m x n) test structures for testing

10   using the p x (m+1) driver lines and 8n receiver lines.

1   28.   The test method of claim 27, wherein:

2   the p levels include odd numbered levels and even numbered levels,

3   each level has 4n receiver lines,

4   and the method further comprises:

5   connecting the respective commonly positioned receiver lines from each of the odd

6   numbered levels to each other, and

7   connecting the respective commonly positioned receiver lines from each of the even

8   numbered levels to each other.

1   29.   A test method, comprising the steps of:

2   (a)   forming circuit paths for at least one layer having n regions, where n is an integer,

3   each region capable of including at least one test structure, at least some of the regions

4   including respective test structures, each comprising a nest of m parallel lines, where m is an

5   integer,

6   (b)   forming m driver lines for the at least one layer;

7   (c)   forming at least 2n receiver lines for the at least one layer;

8   (d)   providing input signals to the respective m parallel lines in each nest using the m

9   driver lines;

10   (e)   measuring output signals from all of the test structures using the at least 2n receiver

11   lines; and

12   (f)   identifying the presence of a short or open circuit defect in any of the nests based on

13   the output signals received by way of the at least 2n receiver lines.

1   30.   The test method of claim 29, wherein the layer has 3n receiver lines, and step (f)

2   includes identifying the presence of a short or open circuit defect in any of the nests based on

3   the output signals received by way of the 3n receiver lines.

1   31.   The test method of claim 29, wherein :

2   the test chip has p layers, each layer having n regions, at least some of the regions in

3   each layer including respective nests of m parallel lines,

4   each of the p layers having m driver lines, the m driver lines connected to provide

5   input signals to the respective m parallel lines in each nest in that respective layer,

6   each layer having at least 2n receiver lines, the at least 2n receiver lines connected to

7   collectively receive output signals from all of the test structures in that respective layer.

1   32.   The test method of claim 31, further comprising connecting receiver lines having

2   corresponding positions in each respective one of the odd numbered layers to each other.

1   33.   The test method of claim 32, wherein the test structures and receiver lines in the odd

2   numbered layers are oriented in a common direction.

1   34.   The test method of claim 32, further comprising connecting receiver lines having

2   corresponding positions in each respective one of the even numbered layers to each other.

1   35.   The test method of claim 32, wherein:

2   the test structures and receiver lines in the odd numbered layers are oriented in a first

3   common direction; and

4   the test structures and receiver lines in the even numbered layers are oriented in a

5   second common direction different from the first common direction.

1   36.   The test method of claim 29, wherein

2   each test structure in the layer is connected to at least one of the driver lines with a

3   first transistor therebetween,

4   each test structure in the layer is connected to at least one of the receiver lines with a

5   second transistor therebetween,

6   step (d) includes performing as one of the group consisting of an outer loop and an

7   inner loop a sequence of successively applying a first voltage to each driver line of the layer,

8   one at a time, while applying a second voltage to all remaining driver lines in the layer;

9   step (e) includes performing as the other of the group consisting of the outer loop and

10   the inner loop a sequence of applying the second voltage to each receiver line of the layer,

11   one at a time, while applying the first voltage to all remaining receiver lines in the layer; and

12   the method further comprises measuring a wafer substrate current to ground each time

13   the second voltage is applied to a different receiver line in step (e).

1   37.   The method of claim 29, wherein:

2   each test structure in the layer is connected to at least one of the driver lines with a

3   first diode therebetween,

4   each test structure in the layer is connected to at least one of the receiver lines with a

5   second diode therebetween,

6   and step (e) includes

7   performing as one of the group consisting of an inner loop and an outer loop a step of

8   successively applying a first signal to each driver line of the level, one at a time, while

9   applying a second signal to all remaining driver lines in the level; and

10   performing as the other of the group consisting of the inner loop and the outer loop a

11   step of measuring a current to ground at each receiver line of the level.

1   38.   A test chip, comprising:

2   at least one layer having a vector of regions, each region capable of including at least

3   one test structure, at least some of the regions including respective test structures,

4   the layer having a plurality of driver lines that provide input signals to the test

5   structures,

6   the layer having a plurality of receiver lines that receive output signals from the test

7   structures,

8   the layer having a plurality of devices for controlling current flow,

9   wherein each test structure is connected to at least one of the driver lines with a first

10   one of the devices therebetween, and

11   each test structure is connected to at least one of the receiver lines with a second one

12   of the devices therebetween, so that each of the test structures can be individually addressed

13   for testing using the driver lines and receiver lines.

1   39.   The test chip of claim 1, wherein each test structure has four or fewer pins.

1   40.   The test chip of claim 8, wherein each test structure has four or fewer pins.

1   41.   The test chip of claim 13, wherein each test structure has four or fewer pins.

1   42.   The test chip of claim 16, wherein each test structure has four or fewer pins.